

CLAIMS

What is claimed is:

Sub A1

1. A method comprising:
 configuring a mode word;
 detecting insertion of a medium into a drive based on the mode word; and
 starting a program on the medium when the insertion is detected.
2. The method of claim 1 wherein configuring the mode word
 comprising:
 configuring the mode word in one of first, second, third, and fourth modes.
3. The method of claim 1 wherein detecting the insertion comprises:
 periodically polling the drive when the mode word is configured in the
 first mode.
4. The method of claim 1 wherein detecting the insertion comprises:
 servicing an interrupt indicating the insertion of the medium when the
 mode is configured in one of the second, third, and fourth modes.
5. The method of claim 1 wherein servicing the interrupt comprises:

servicing the interrupt generated by a polling circuit in a chipset when the mode is configured in one of the second and third modes, the polling circuit detecting the insertion of the medium.

6. The method of claim 5 wherein servicing the interrupt comprises:

checking a status bit set by the polling circuit when the mode is configured in the second mode; and

updating a flag in a memory based on the status bit; and

responding to a poll request by an operating system.

7. The method of claim 6 wherein responding comprises:

reading the flag from the memory.

8. The method of claim 4 wherein servicing the interrupt comprises:

servicing the interrupt generated by the drive.

9. A method comprises:

checking a status bit in response to an interrupt generated by a polling circuit in a chipset, the polling circuit detecting insertion of a medium into a drive;

updating a flag in a memory based on the status bit; and

responding to a poll request by an operating system.

10. The method of claim 9 wherein responding comprises:

2 reading the flag from the memory.

1 11. The method of claim 9 wherein checking the status comprises:
 2 checking the status bit set by the polling circuit upon detecting the
 3 insertion of the medium.

1 12. The method of claim 9 further comprises:
 2 loading a program on the medium into a memory; and
 3 executing the program.

1 13. A computer program product comprising:
 2 a machine useable medium having computer program code embedded
 3 therein, the computer program product having:
 4 computer readable program code to configure a mode word;
 5 computer readable program code to detect insertion of a medium into a
 6 drive based on the mode word; and
 7 computer readable program code to start a program on the medium when
 8 the insertion is detected.

1 14. The computer program product of claim 13 wherein the computer
 2 readable program code to configure the mode word comprising:
 3 computer readable program code to configure the mode word in one of
 4 first, second, third, and fourth modes.

1 15. The computer program product of claim 13 wherein the computer
2 readable program code to detect the insertion comprises:

3 computer readable program code to periodically poll the drive when the
4 mode word is configured in the first mode.

1 16. The computer program product of claim 13 wherein the computer
2 readable program code to detect the insertion comprises:

3 computer readable program code to service an interrupt indicating the
4 insertion of the medium when the mode is configured in one of the second, third,
5 and fourth modes.

1 17. The computer program product of claim 13 wherein the computer
2 readable program code to service the interrupt comprises:

3 computer readable program code to service the interrupt generated by a
4 polling circuit in a chipset when the mode is configured in one of the second and
5 third modes, the polling circuit detecting the insertion of the medium.

1 18. The computer program product of claim 17 wherein the computer
2 readable program code to service the interrupt comprises:

3 computer readable program code to check a status bit set by the polling
4 circuit when the mode is configured in the second mode;

5 computer readable program code to update a flag in a memory based on
6 the status bit; and

7 computer readable program code to respond to a poll request by an
8 operating system.

1 19. The computer program product of claim 18 wherein the computer
2 readable program code to respond comprises:

3 computer readable program code to read the flag from the memory.

1 20. The computer program product of claim 16 wherein the computer
2 readable program code to service the interrupt comprises:

3 computer readable program code to service the interrupt generated by the
4 drive.

1 21. A computer program product comprising:

2 a machine useable medium having computer program code embedded
3 therein, the computer program product having:

4 computer readable program code to check a status bit in response to an
5 interrupt generated by a polling circuit in a chipset, the polling circuit detecting
6 insertion of a medium into a drive;

7 computer readable program code to update a flag in a memory based on
8 the status bit; and

9 computer readable program code to respond to a poll request by an
10 operating system.

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1 22. The computer program product of claim 21 wherein the computer
2 readable program code to respond comprises:

3 computer readable program code to read the flag from the memory.

1 23. The computer program product of claim 21 wherein the computer
2 readable program code to check the status bit comprises:

3 computer readable program code to check the status bit set by the polling
4 circuit upon detecting the insertion of the medium.

1 24. The computer program of claim 21 further comprising:

2 computer readable program code to load a program on the medium into a
3 memory; and

4 computer readable program code to execute the program.

1 25. A system comprising:

2 a processor;

3 a chipset coupled to the processor to control a drive; and

4 a memory coupled to the processor to store instruction code, the
5 instruction code, when executed by the processor, causing the processor to:

6 configure a mode word,

7 detect insertion of a medium into a drive based on the mode word,

8 and

9 start a program on the medium when the insertion is detected.

1 26. The system of claim 25 wherein the instruction code causing the
2 processor to configure the mode word causes the processor to:

3 configure the mode word in one of first, second, third, and fourth modes.

1 27. The system of claim 25 wherein the instruction code causing the
2 processor to detect insertion causes the processor to:

3 periodically poll the drive when the mode word is configured in the first
4 mode.

1 28. The system of claim 25 wherein the instruction code causing the
2 processor to detect insertion causes the processor to:

3 service an interrupt indicating the insertion of the medium when the mode
4 is configured in one of the second, third, and fourth modes.

1 29. The system of claim 25 wherein the instruction code causing the
2 processor to service the interrupt causes the processor to:

3 service the interrupt generated by a polling circuit in the chipset when the
4 mode is configured in one of the second and third modes, the polling circuit
5 detecting the insertion of the medium.

1 30. The system of claim 29 wherein the instruction code causing the
2 processor to service the interrupt causes the processor to:

3 check a status bit set by the polling circuit when the mode is configured in
4 the second mode;

5 update a flag in a memory based on the status bit, and
6 respond to a poll request by an operating system.

1 31. A system comprising:

2 a processor;

3 a chipset coupled to the processor to control a drive, the chipset having a
4 polling circuit to detect insertion of a medium into the drive; and

5 a memory coupled to the processor to store instruction code, the
6 instruction code, when executed by the processor, causing the processor to:

7 check a status bit in response to an interrupt generated by the
8 polling circuit when the insertion is detected,

9 update a flag in a memory based on the status bit, and

10 respond to a poll request by an operating system.

1 32. The system of claim 31 wherein the instruction code causing the
2 processor to respond causes the processor to:

3 read the flag from the memory.

1 33. The system of claim 31 wherein the instruction code causing the
2 processor to check the status bit causes the processor to:

1 34. The system of claim 31 wherein the instruction code further
2 causing the processor to:

4 execute the program.

[illegible]